Intel® E7520/E7320 Chipset Memory Controller Hub (MCH) and Intel® 6700PXH 64-Bit PCI Hub

Thermal/Mechanical Design Guide for Embedded Applications

February 2007

Reference Number: 304387-004

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Revision History

Date	Revision	Description
February 2007	004	Changed section Section 7.1.
December 2005	003	Changed values in Table 2. Updated Figure 21 and Figure 22. Added Figure 23.
February 2005	002	Added E7320 TDP values
October 2004	001	Initial Release

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1.0 Introduction

As the complexity of computer systems increases, so does the power dissipation of the components. Care must be taken to ensure that the additional power is properly dissipated. Typical methods to improve heat dissipation include selective use of ducting and/or passive heat sinks.

The goals of this document are as follows:

- To specify the operating limits of the Intel® E7520/E7320 Chipset Memory Controller Hub (MCH) and Intel® 6700PXH 64-Bit PCI Hub components.
- To describe a reference thermal solution that meets the thermal specification of the Intel E7520/E7320 Chipset MCH and Intel 6700PXH 64-Bit PCI Hub components.

Properly designed thermal solutions provide adequate cooling to maintain the Intel E7520/E7320 Chipset MCH and Intel 6700PXH 64-Bit PCI Hub die temperatures at or below thermal specifications. This is accomplished by ensuring adequate local airflow and minimizing the die to local-ambient thermal resistance. By maintaining the Intel E7520/E7320 Chipset MCH and Intel 6700PXH 64-Bit PCI Hub die temperature at or below the specified limits, a system designer can ensure the proper functionality, performance, and reliability of the chipset. Operation outside the functional limits can degrade system performance and may cause permanent changes in the operating characteristics of the component.

The simplest and most cost-effective method is to improve the inherent system cooling characteristics through careful design and placement of fans, vents, and ducts. When additional cooling is required, component thermal solutions may be implemented in conjunction with system thermal solutions. The size of the fan or heat sink can be varied to balance size and space constraints with acoustic noise.

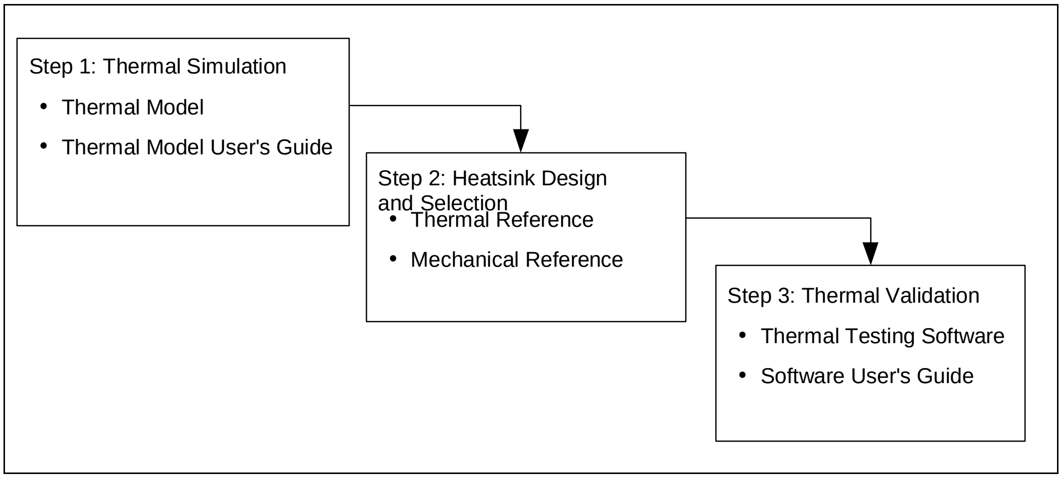
This document addresses thermal design and specifications for the Intel E7520/E7320 Chipset chipset MCH and PXH components only. For thermal design information on other chipset components, refer to the respective component datasheet. For the Intel® 6300ESB I/O Controller Hub (ICH), refer to the *Intel® 6300ESB I/O Controller Hub Thermal Design Guidelines*.

Note: Unless otherwise specified, the term “MCH” refers to the Intel E7520/E7320 Chipset MCH, and the term “PXH” refers to the Intel 6700PXH 64-Bit PCI Hub.

1.1 Design Flow

To develop a reliable, cost-effective thermal solution, several tools are available to the system designer. Figure 1 illustrates the design process implicit to this document and the tools appropriate for each step.

Figure 1. Thermal Design Process



1.2 Definition of Terms

Table 1. Definition of Terms

Term	Definition
FC-BGA	Flip Chip Ball Grid Array. A ball grid array packaging technology where the die is exposed on the package substrate.
Intel® 6300ESB I/O Controller Hub	I/O Controller Hub. The chipset component that contains the primary PCI interface, PCI-X interfaces, LPC interface, USB, ATA-100, and other legacy functions.
MCH	Memory Controller Hub. The chipset component that contains the processor interface, the memory interface, and the hub interface.
PXH	PCI-X Hub. The chipset component that performs PCI bridging functions between the PCI Express interface and the PCI Bus.
T_{CASE_MAX}	Maximum die temperature allowed. This temperature is measured at the geometric center of the top of the package die.
T_{CASE_MIN}	Minimum die temperature allowed. This temperature is measured at the geometric center of the top of the package die.
TDP	Thermal Design Power. Thermal solutions should be designed to dissipate this target power level.
T_{LA}	Local ambient temperature. This is the temperature measured inside the chassis, approximately 1" upstream of a component heatsink.
Psi ca (Ψ_{CA})	Case-to-ambient thermal characterization parameter. A measure of heat sink thermal performance using total package power. Defined as (T_{CASE} - T_{LA}) / Total Package Power

1.3 Reference Documents

The reader of this specification must also be familiar with material and concepts presented in the following documents:

- *Intel® E7520/Intel® E7320 /Intel® E7525 Chipset Memory Controller Hub (MCH) Thermal Design Guidelines (TDG)*
- *Intel® 6700PXH 64-Bit PCI Hub Thermal Design Guidelines*
- *Intel® 6300ESB I/O Controller Hub Thermal and Mechanical Design Guide*
- *Intel® 6300ESB I/O Controller Hub Datasheet*
- *Intel® 6700PXH 64-Bit PCI Hub Datasheet*
- *Intel® E7520/E7320 Chipset MCH Datasheet*
- *Intel® Xeon™ Processor with 800 MHz System Bus Thermal/Mechanical Design Guidelines*
- *Low-Voltage Intel® Xeon™ Processor with 800 MHz System Bus in Embedded Applications Thermal Design Guidelines*
- *Intel® Xeon™ Processor with 800 MHz System Bus Datasheet*
- *Various System Thermal Design Suggestions (http://www.formfactors.org)*
- *Low-Voltage Intel® Xeon™ Processor with 800 MHz System Bus Datasheet*
- *Intel® Pentium® M Processor on 90 nm Process with 2-MB L2 Cache for Embedded Applications Thermal Design Guide*

Note: Unless otherwise noted, these documents are available through your Intel field sales representative.

2.0 Packaging Technology

The MCH utilizes a 42.5 mm × 42.5 mm, 10-layer FC-BGA package (see Figure 2, Figure 3, and Figure 4). The PXH utilizes a 31 mm × 31 mm, 8-layer FC-BGA package (see Figure 5, Figure 6, and Figure 7). For information on the Intel® 6300ESB I/O Controller Hub package, refer to the *Intel® 6300ESB I/O Controller Hub Thermal and Mechanical Design Guidelines*.

Figure 2. MCH Package Dimensions (Top View)

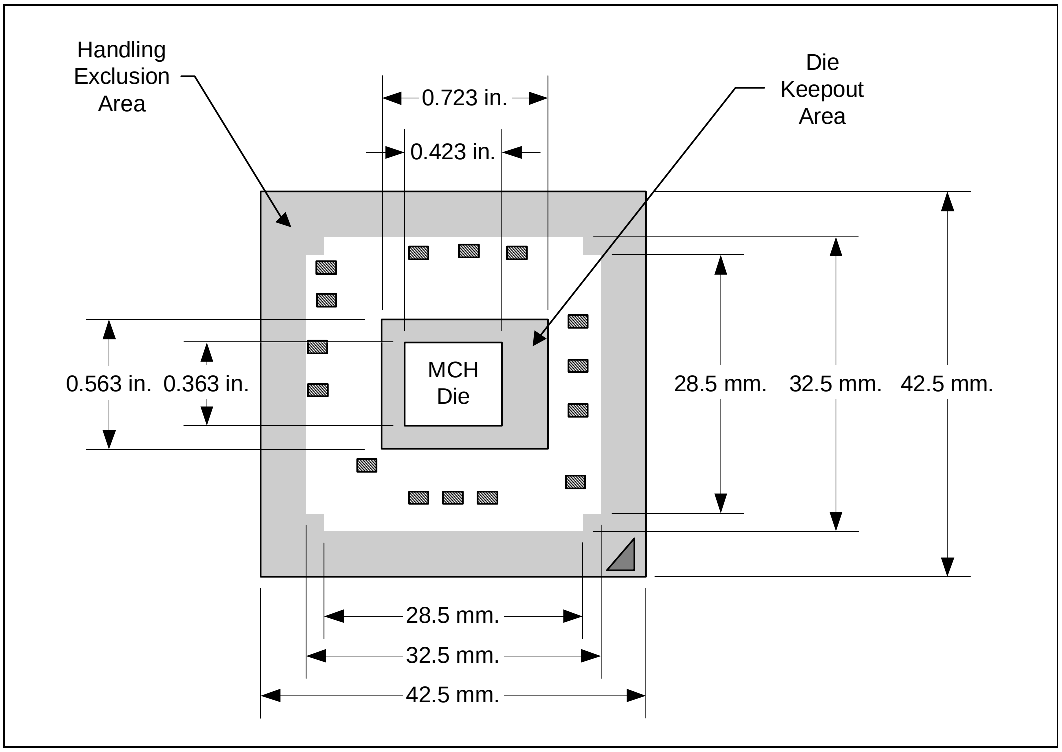
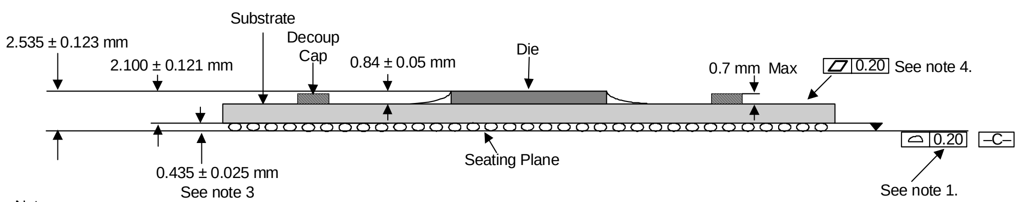
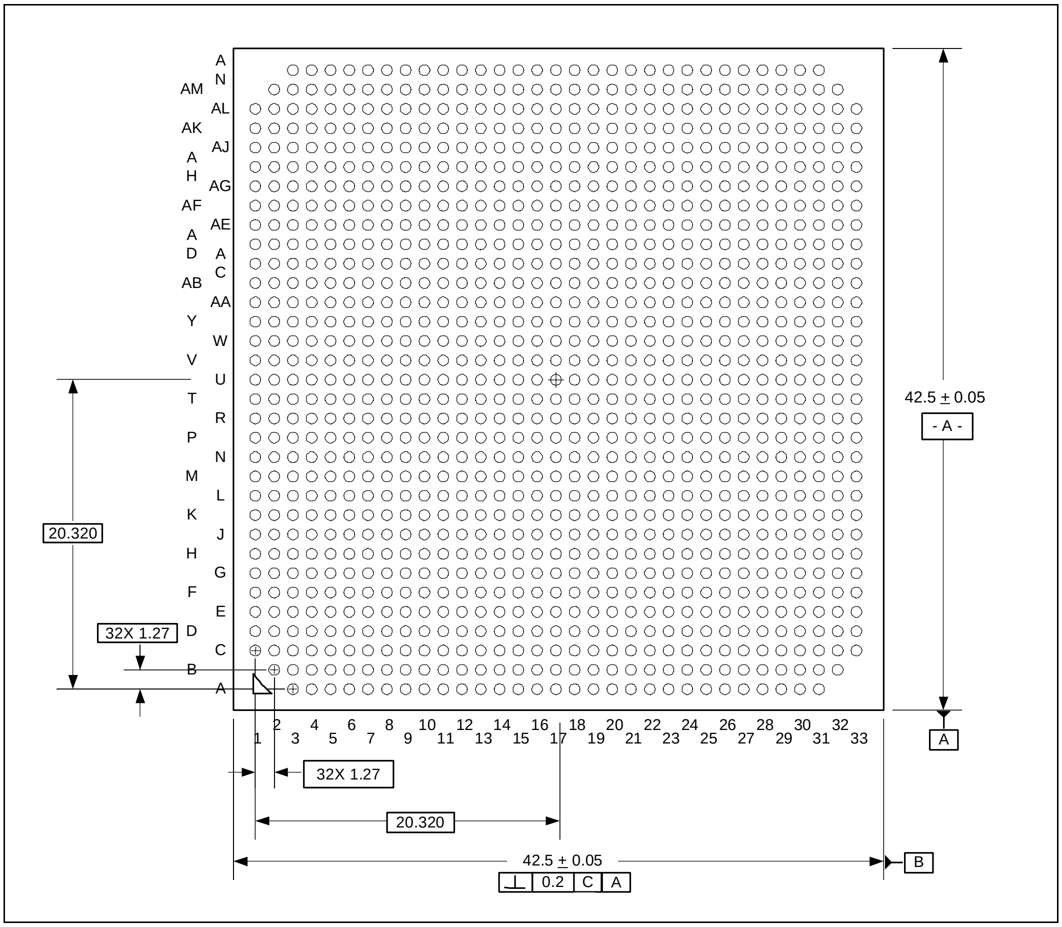


Figure 3. MCH Package Dimensions (Side View)



Notes:
1. Primary datum -C- and seating plan are defined by the spherical crowns of the solder balls (shown before motherboard attach)
2. All dimensions and tolerances conform to ANSI Y14.5M-1994
3. BGA has a pre-SMT height of 0.5mm and post-SMT height of 0.41-0.46mm
4. Shown before motherboard attach; FCBGA has a convex (dome shaped) orientation before reflow and is expected to have a slightly concave (bowl shaped) orientation after reflow

Figure 4. MCH Package Dimensions (Bottom View)



NOTES:

1. All dimensions are in millimeters.
2. All dimensions and tolerances conform to ANSI Y14.5M-1994.

Figure 5. PXH Package Dimensions (Top View)

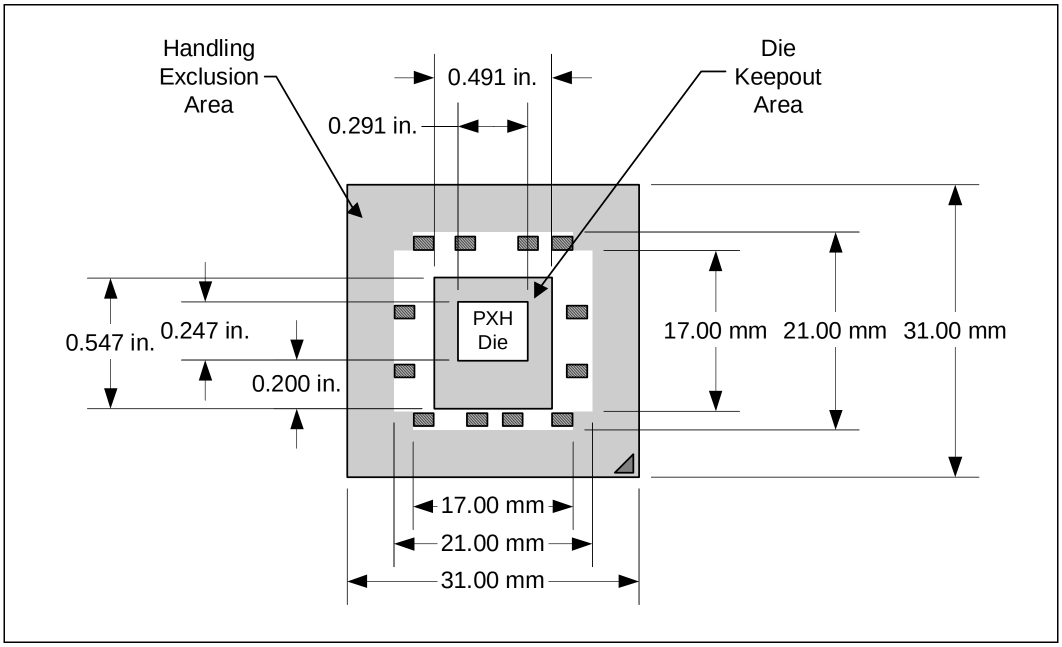
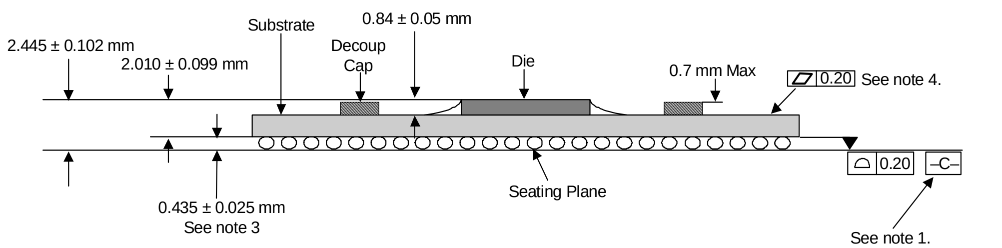
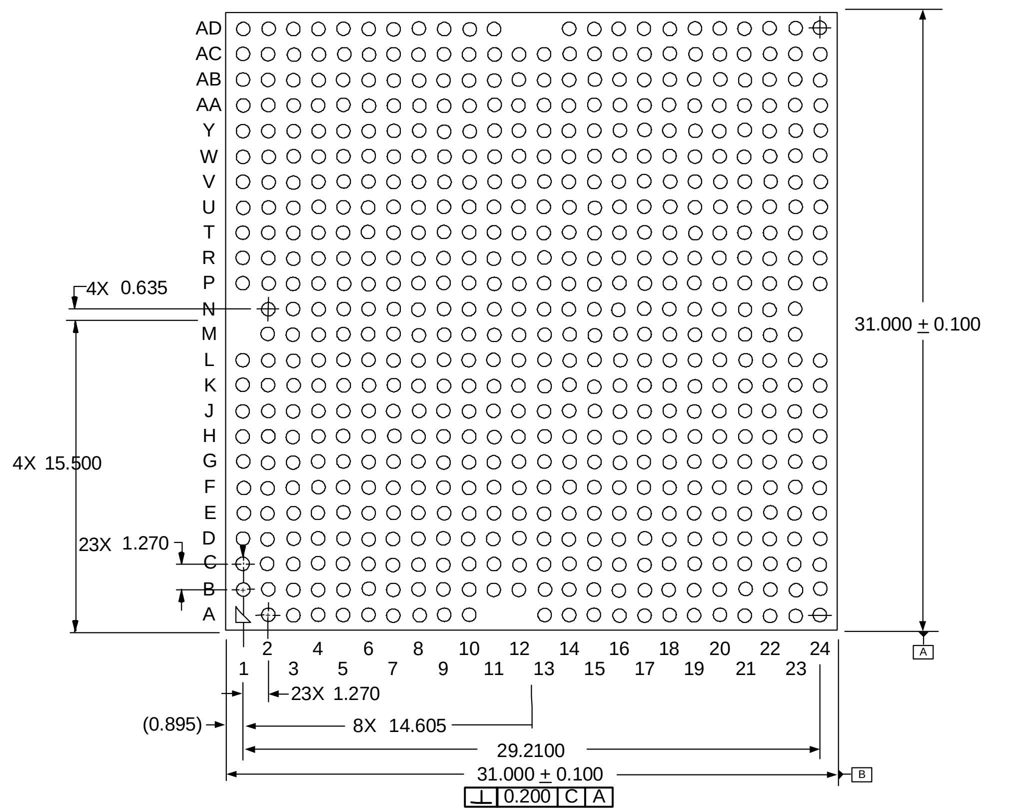


Figure 6. PXH Package Dimensions (Side View)



Notes:
1. Primary datum -C- and seating plan are defined by the spherical crowns of the solder balls (shown before motherboard attach)
2. All dimensions and tolerances conform to ANSI Y14.5M-1994
3. BGA has a pre-SMT height of 0.5mm and post-SMT height of 0.41-0.46mm
4. Shown before motherboard attach; FCBGA has a convex (dome shaped) orientation before reflow and is expected to have a slightly concave (bowl shaped) orientation after reflow

Figure 7. PXH Package Dimensions (Bottom View)



2.1 Package Mechanical Requirements

The MCH and PXH packages each have an exposed bare die that is capable of sustaining a maximum static normal load of 15 lbf. The packages are ***not*** capable of sustaining a dynamic or static compressive load applied to any edge of the bare die. These mechanical load limits must not be exceeded during heat sink installation, mechanical stress testing, standard shipping conditions and/or any other use condition.

Note: The heat sink attach solutions must not include continuous stress onto the chipset package with the exception of a uniform load to maintain the heat sink-to-package thermal interface.

Note: These specifications apply to uniform compressive loading in a direction perpendicular to the bare die top surface.

Note: These specifications are based on limited testing for design characterization. Loading limits are for the package only.

3.0 Thermal Simulation

Intel provides thermal simulation models of the MCH and PXH and associated thermal model user guides to aid system designers in simulating, analyzing, and optimizing their thermal solutions in an integrated, system-level environment. The models are for use with the commercially available Computational Fluid Dynamics (CFD)-based thermal analysis tools Flotherm* (version 3.1 or higher) by Flomerics, Inc. or Icepak* by Fluent, Inc. Contact your Intel representative to order the thermal models and associated user's guides.

4.0 Thermal Specifications

4.1 Thermal Design Power (TDP)

Analysis indicates that real applications are unlikely to cause the MCH or PXH components to consume maximum power dissipation for sustained time periods. Therefore, to arrive at a more realistic power level for thermal design purposes, Intel characterizes power consumption based on known platform benchmark applications. The resulting power consumption is referred to as the Thermal Design Power (TDP). TDP is the target power level that the thermal solutions should be designed to. TDP is not the maximum power that the chipset can dissipate.

TDP specifications for the MCH and PXH components are listed in Table 2 and Table 3. Flip chip ball grid array (FC-BGA) packages have poor heat transfer capability into the board and have minimal thermal capability without a thermal solution. Intel recommends that system designers plan for a heat sink when using the PXH component.

4.2 Die Temperature

To ensure proper operation and reliability of the MCH and PXH, the die temperatures must be at or below the values specified in Table 2 and Table 3. System and/or component-level thermal solutions are required to maintain die temperatures below the maximum case specifications while dissipating the TDP for that component. Refer to Section 5.0, “Thermal Metrology” on page 17 for guidelines on accurately measuring package die temperatures.

Table 2. Intel® E7520/E7320 Chipset MCH Thermal Specifications

Parameter	Value	FSB Speed	Component	Notes
T_{CASE_MAX}	105°C	N/A	E7520 and E7320	All cases
T_{CASE_MIN}	5°C	N/A	E7520 and E7320	All cases
$TDP_{Dual\ Channel}$	10.0W	800 MHz	E7520	DDRI-266
$TDP_{Single\ Channel}$	8.0W	800 MHz	E7520	DDRI-266
$TDP_{Dual\ Channel}$	10.0W	800 MHz	E7520	DDRI-333
$TDP_{Single\ Channel}$	8.5W	800 MHz	E7520	DDRI-333
$TDP_{Dual\ Channel}$	9.7W	800 MHz	E7520	DDR2-400
$TDP_{Single\ Channel}$	9.1W	800 MHz	E7520	DDR2-400
$TDP_{Dual\ Channel}$	9.3W	667 MHz	E7520	DDR2-400
$TDP_{Single\ Channel}$	8.7W	667 MHz	E7520	DDR2-400
$TDP_{Dual\ Channel}$	9.0W	533 MHz	E7520	DDR2-400
$TDP_{Single\ Channel}$	8.4W	533 MHz	E7520	DDR2-400
$TDP_{Dual\ Channel}$	8.8W	400 MHz	E7520	DDR2-400
$TDP_{Single\ Channel}$	8.2W	400 MHz	E7520	DDR2-400
$TDP_{Dual\ Channel}$	7.5W	400 MHz	E7320	DDR2-400
$TDP_{Single\ Channel}$	6.9W	400 MHz	E7320	DDR2-400

NOTE: These specifications are based on silicon characterization.

Table 3. Intel® 6700PXH 64-Bit PCI Hub Thermal Specifications

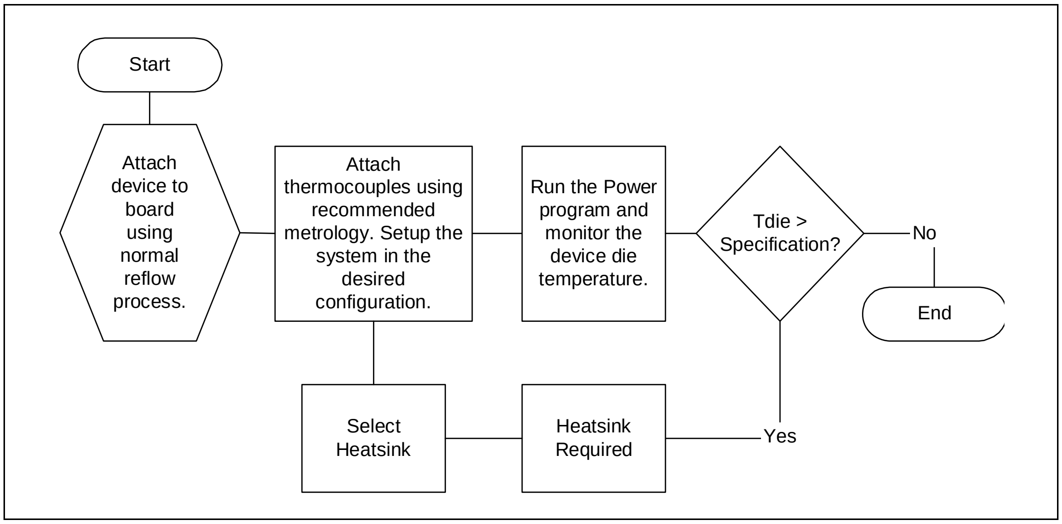
Parameter	Maximum	Notes
T_{CASE}	105 °C	All cases
T_{CASE_MIN}	5 °C	All cases
TDP Segment A @ 66 MHz and Segment B @ 66 MHz	9.0 W	
TDP Segment A @ 100 MHz and Segment B @ 100 MHz	8.9 W	
TDP Segment A @ 133 MHz and Segment B @ 133 MHz	8.6 W	
TDP Segment A @ 66 MHz and Segment B @ 100 MHz	8.9 W	
TDP Segment A @ 66 MHz and Segment B @ 133 MHz	8.8 W	
TDP Segment A @ 100 MHz and Segment B @ 133 MHz	8.7 W	

NOTE: These specifications are based on silicon characterization.

5.0 Thermal Metrology

The system designer must make temperature measurements to accurately determine the thermal performance of the system. Intel has established guidelines for proper techniques to measure the component die temperatures. Section 5.1 provides guidelines on how to accurately measure the component die temperatures. Section 5.2 contains information on running an application program that will emulate the anticipated thermal design power. The flowchart in Figure 8 offers useful guidelines for thermal performance and evaluation.

Figure 8. Thermal Solution Decision Flowchart



5.1 Die Temperature Measurements

To ensure functionality and reliability, the component T_{CASE} must be maintained at or below the maximum temperature specification as noted in Table 2 and Table 3. The surface temperature at the geometric center of the die corresponds to T_{CASE}. Measuring T_{CASE} requires special care to ensure an accurate temperature measurement.

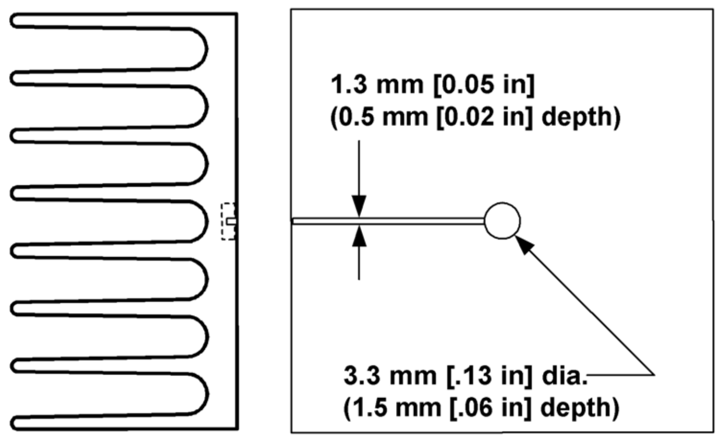
Temperature differences between the temperature of a surface and the surrounding local ambient air can introduce errors in the measurements. The measurement errors could be due to a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation and/or convection, conduction through thermocouple leads, or contact between the thermocouple cement and the heat sink base (if a heat sink is used). To maximize measurement accuracy, only the 0° thermocouple attach approach is recommended.

5.1.1 0° Angle Attach Methodology

1. Mill a 3.3 mm (0.13”) diameter and 1.5 mm (0.06”) deep hole centered on the bottom of the heat sink base.
2. Mill a 1.3 mm (0.05”) wide and 0.5 mm (0.02”) deep slot from the centered hole to one edge of the heat sink (see Figure 9).
3. Attach Thermal Interface Material (TIM) to the bottom of the heat sink base.

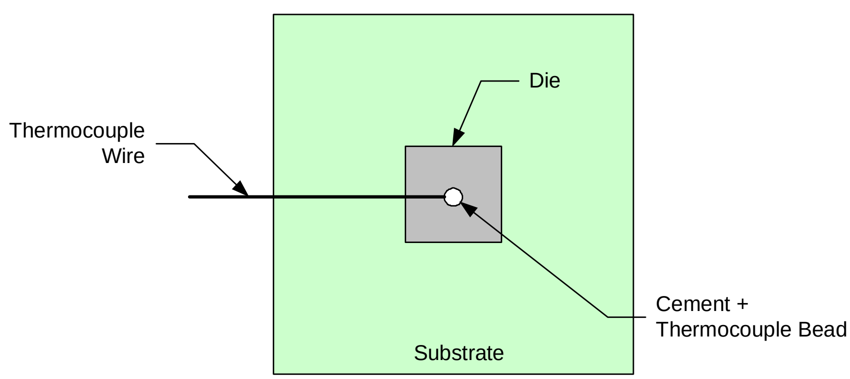
4. Cut out portions of the TIM to make room for the thermocouple wire and bead. The cutouts should match the slot and hole milled into the heat sink base.
5. Attach a 36 gauge or smaller calibrated K-type thermocouple bead to the center of the top surface of the die using a high thermal conductivity cement. During this step, ensure no contact is present between the thermocouple cement and the heat sink base because it may affect the thermocouple reading. **It is critical that the thermocouple bead makes contact with the die** (see Figure 10).
6. Attach the heat sink assembly to the MCH and route thermocouple wires out through the milled slot.

Figure 9. 0° Angle Attach Heat Sink Modifications



NOTE: Not to scale.

Figure 10. 0° Angle Attach Methodology (Top View)



NOTE: Not to scale.

5.2 Power Simulation Software

The power simulation software is a utility designed to dissipate the TDP on an Intel® E7520/E7320 Chipset MCH when used in conjunction with the Intel® Xeon™ Processor with 800 MHz System Bus, or the Low-Voltage Intel® Xeon™ Processor with 800 MHz System Bus and the Intel® Pentium® M Processor on 90 nm Process with 2-MB L2 Cache. The combination of the above-mentioned processor(s) and the higher bandwidth capability of the Intel E7520/E7320 Chipset enable higher levels of system performance. To assess the thermal performance of the chipset MCH thermal solution under worst-case realistic application conditions, Intel has developed a software utility that operates the chipset at near worst-case power dissipation.

The power simulation software should only be used to test customer thermal solutions at or near the thermal design power. Figure 8 shows a decision flowchart for determining thermal solution needs. Real-world applications may exceed the thermal design power limit for transient time periods. For power supply current requirements under these transient conditions, refer to each component's datasheet for the ICC (Max Power Supply Current) specification. Contact your Intel field sales representative to order the Power Utility and Software User’s Guide.

6.0 Reference Thermal Solution

Intel has developed embedded reference thermal solutions designed to meet the cooling needs of the Intel® E7520/E7320 Chipset MCH and Intel® 6700PXH 64-Bit PCI Hub under worst-case conditions. This chapter describes the overall requirements for the reference thermal solution including critical-to-function dimensions, operating environment, and validation criteria. Other chipset components may or may not need attached thermal solutions, depending on your specific system local-ambient operating conditions. For information on the Intel® 6300ESB I/O Controller Hub, refer to thermal specification in the Intel® 6300ESB I/O Controller Hub *Thermal and Mechanical Design Guide*.

6.1 Operating Environment and Thermal Performance

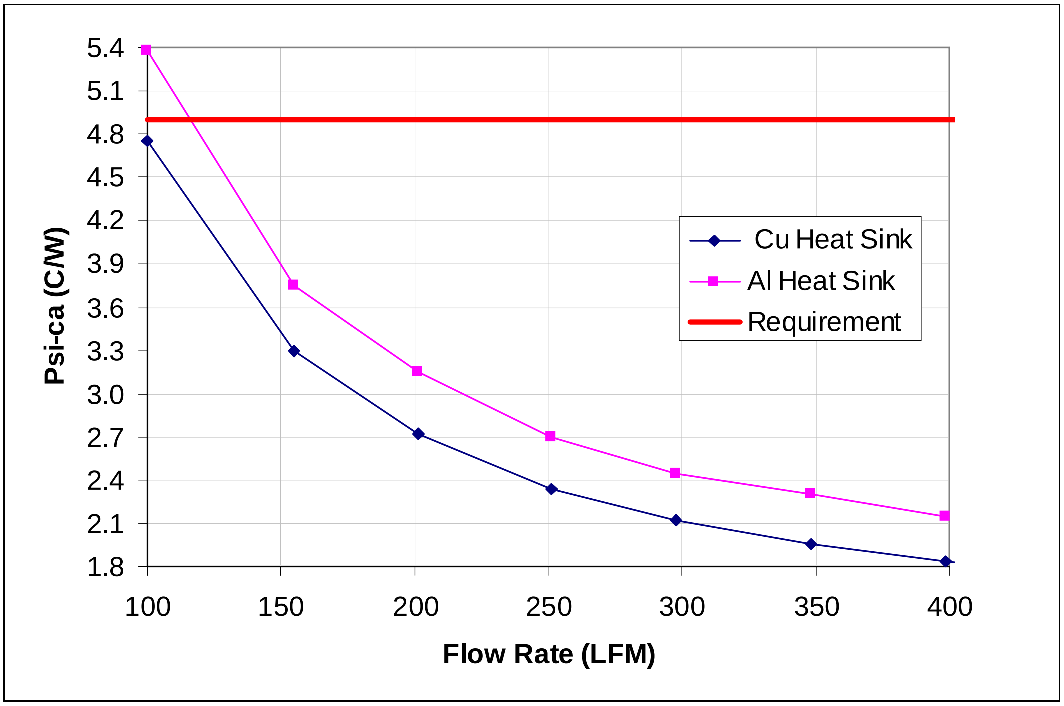
Reference thermal solutions have been designed for the MCH and the PXH. This document details solutions that are compatible with the AdvancedTCA* form factor. Refer to the *Intel® E7520/Intel® E7320/Intel® E7525 Chipset Memory Controller Hub (MCH) Thermal Design Guidelines* and the Intel® 6700PXH 64-Bit PCI Hub/*Intel® 6702PXH 64-Bit PCI Hub Thermal Design Guidelines* for additional reference solutions targeted for 1U, 2U, and larger form factors.

The reference thermal solutions compatible with AdvancedTCA* were designed assuming a maximum local-ambient temperature (TLA) of 55 ºC with a minimum airflow velocity directly upstream of the heatsink of less than 100 LFM for the MCH and PXH solutions. Assuming these boundary conditions are met, the reference thermal solutions will meet the thermal specifications for the MCH and PXH in all memory and Hub Interface configurations. See Figure 11 and Figure 12 for plots of the measured thermal performance of the reference thermal solutions versus approach velocity. Since this data was measured at sea level, a correction factor would be required to estimate thermal performance at other altitudes. Refer to Table 4 for the required Ψ_{CA} heat sink performances for the MCH and PXH.

Table 4. Ψ_{CA} Maximum vs. Device and Configuration

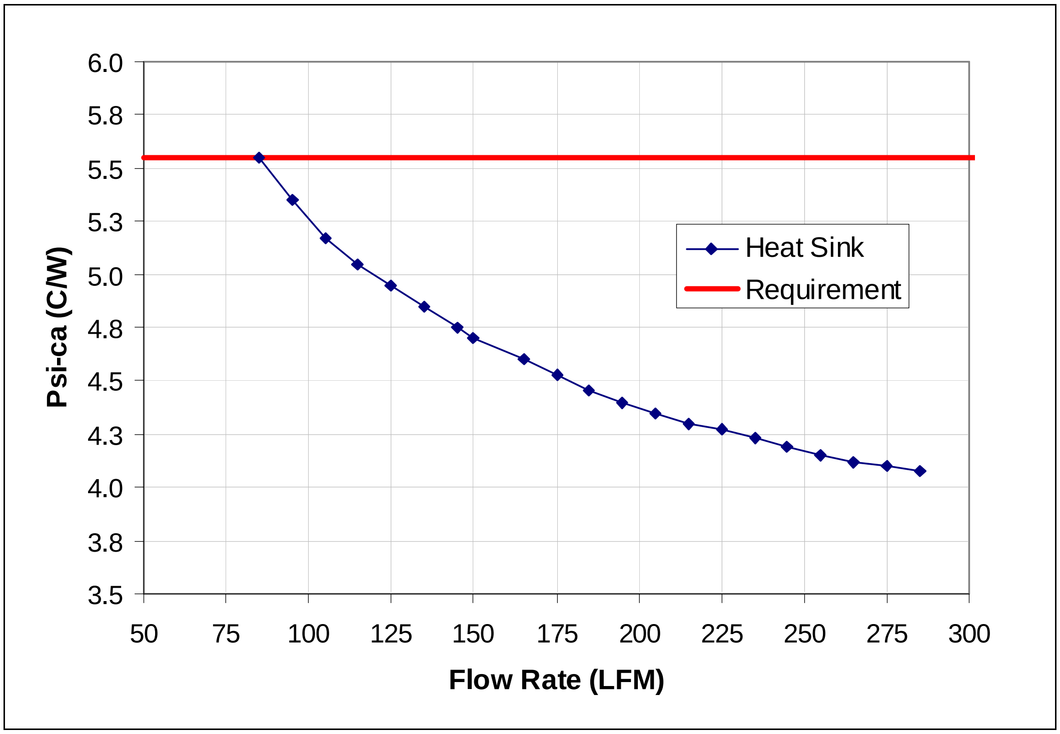
Device	Ψca Max (ºC/W) at T_{LA} = 55ºC†
Intel® E7520 Chipset MCH in DDR1-266 dual-channel memory configuration	5.0 °C/W
Intel® 6700PXH 64-Bit PCI Hub in Segment A @ 66 MHz & Segment B @ 66 MHz configuration	5.6 °C/W
† T_{LA} is defined as the local (internal) ambient temperature measured approximately 1” upstream of the chipset.	

Figure 11. Intel® E7520/E7320 Chipset MCH Reference Heat Sink Measured Thermal Performance Versus Approach Velocity



The MCH reference heat sink has been designed to use either copper or aluminum as the heat sink material. The copper version provides the best cooling while the aluminum version will cost less. Both will satisfy the boundary conditions with less than 150 LFM inlet velocity.

Figure 12. Intel® 6700PXH 64-Bit PCI Hub Reference Heat Sink Measured Thermal Performance Versus Approach Velocity

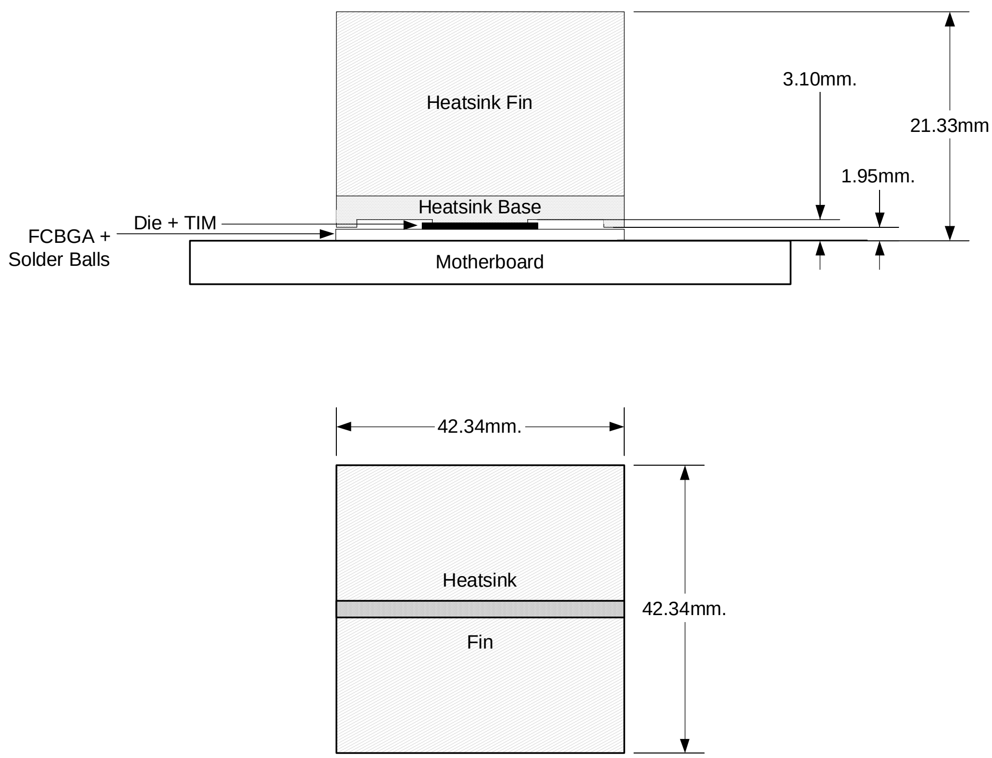


6.2 Mechanical Design Envelope

Though each design may have unique mechanical volume and height restrictions or implementation requirements, the keep-out envelope for MCH using the reference thermal solution is shown in Figure 13. The keep out envelope for the PXH is shown in Figure 14. These constraints assume the use of the single-slot AdvancedTCA* form factor.

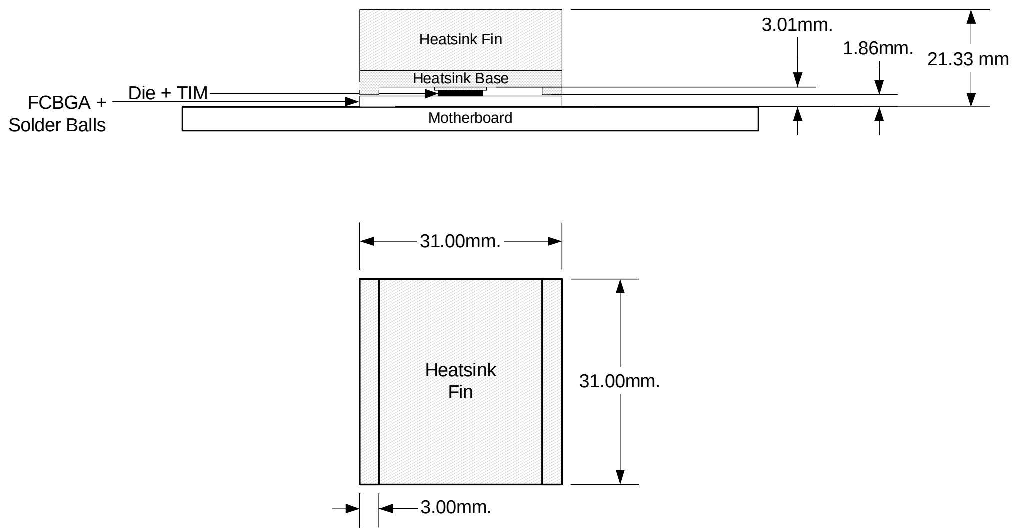
When using heat sinks that extend beyond the MCH or PXH reference heat sink envelopes shown in Figure 13 and Figure 14, any motherboard components placed between the underside of the heatsink and motherboard cannot exceed 2.286 mm [0.090”] in height.

Figure 13. Reference Heat Sink Volumetric Envelope for the Intel® E7520/E7320 Chipset MCH in the AdvancedTCA* Form Factor



NOTE: Not to scale.

Figure 14. Reference Heat Sink Volumetric Envelope for the Intel® 6700PXH 64-Bit PCI Hub in the AdvancedTCA* Form Factor

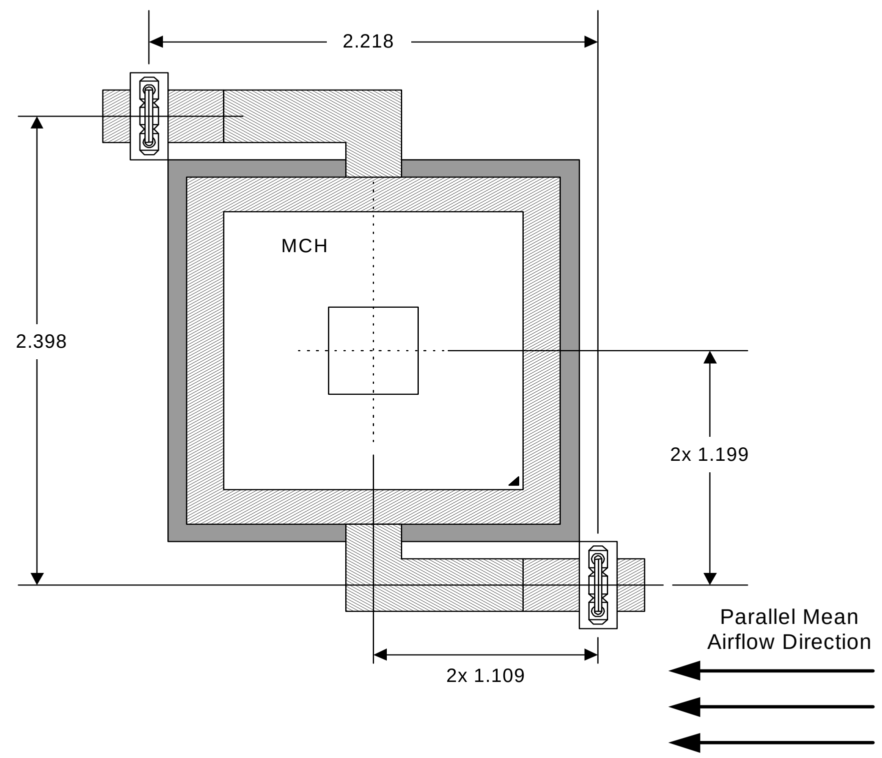


NOTE: Not to scale.

6.3 Board-Level Components Keep-out Dimensions

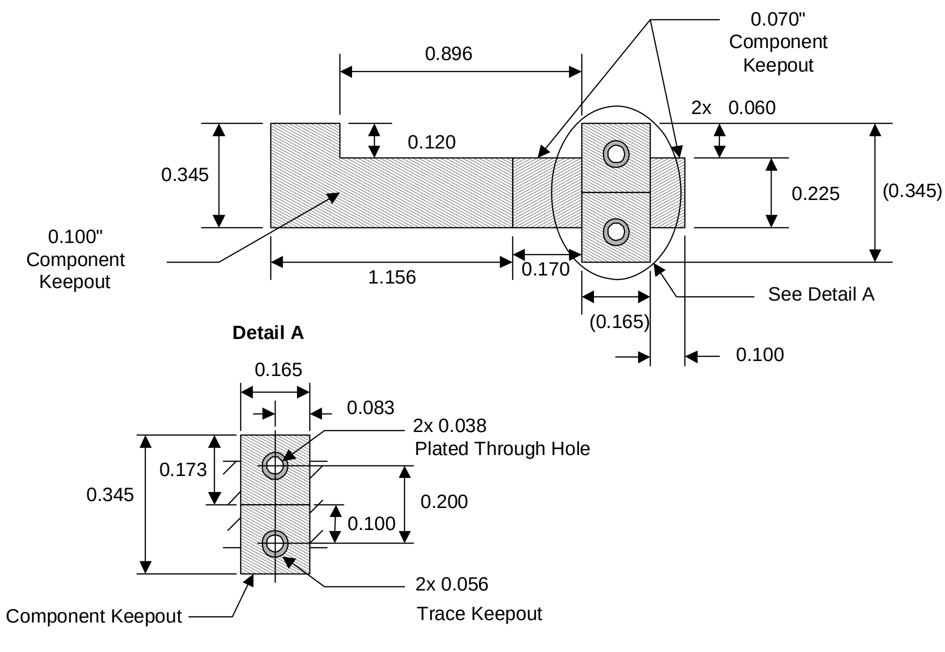
The locations of hole patterns and keep-out zones for the MCH and PXH reference thermal solutions are shown in Figure 15, Figure 16, Figure 17, and Figure 18.

Figure 15. MCH Torsional Clip Heat Sink Board Component Keep-out



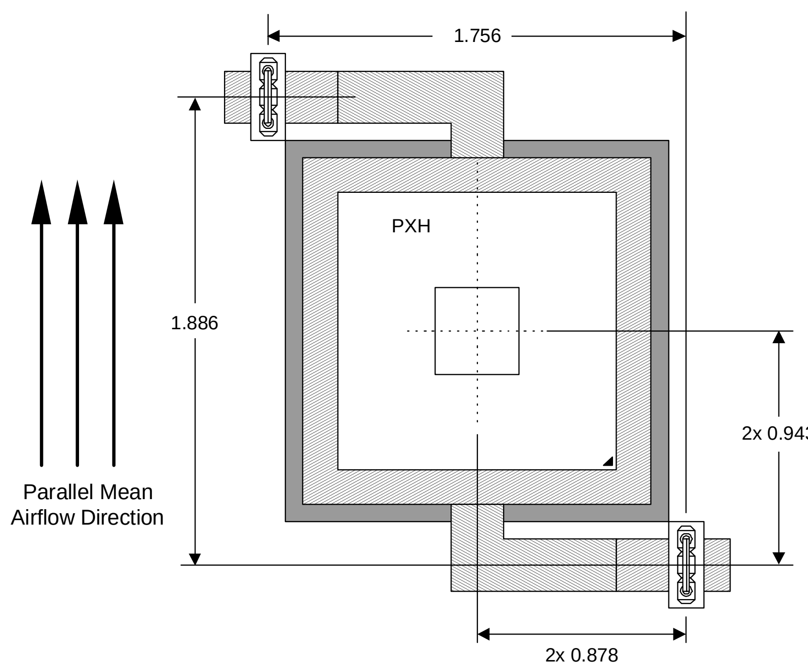
NOTE: All dimensions are in inches.

Figure 16. Intel® E7520/E7320 Chipset MCH Retention Mechanism Component Keep-out Zones



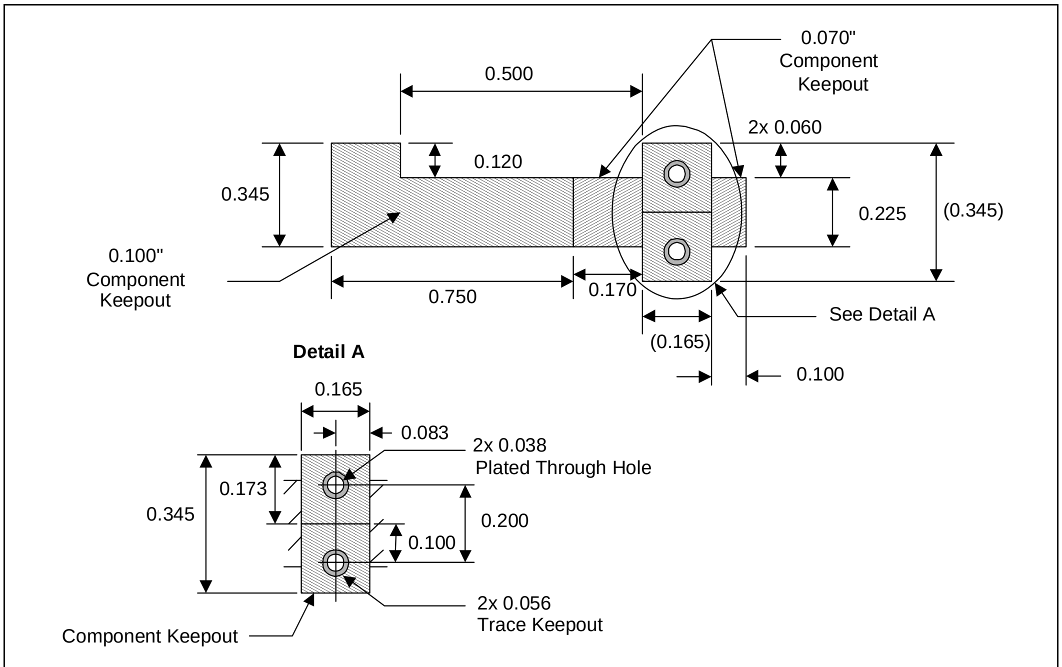
NOTE: All dimensions are in inches.

Figure 17. Intel® 6700PXH 64-Bit PCI Hub Torsional Clip Heat Sink Board Component Keep-out



NOTE: All dimensions are in inches.

Figure 18. Intel® 6700PXH 64-Bit PCI Hub Retention Mechanism Component Keep-out Zones



NOTE: All dimensions are in inches.

6.4 Torsional Clip Heat Sink Thermal Solution Assembly

The MCH and PXH heat sinks are attached to the board using a clip with each end hooked through and anchor soldered to the board. Figure 19 shows the MCH reference thermal solution assembly and Figure 20 shows the PXH reference thermal solution assembly.

Full mechanical drawings of the MCH and PXH thermal solution assemblies and the corresponding heat sink clips are provided in Section 8.0. Section 7.0 contains vendor information for each thermal solution component.

Figure 19. Intel® E7520/E7320 Chipset MCH Reference Thermal Solution Assembly

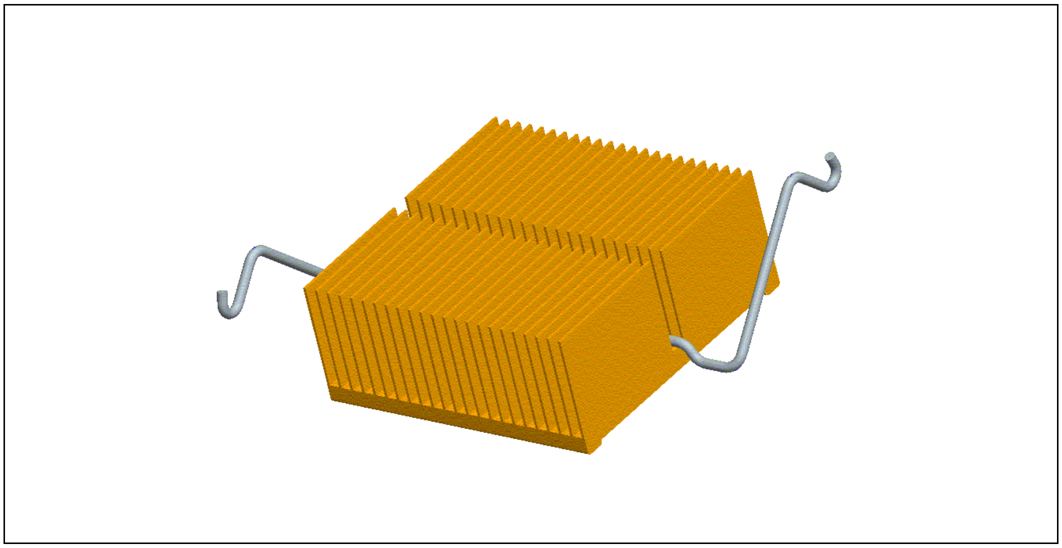
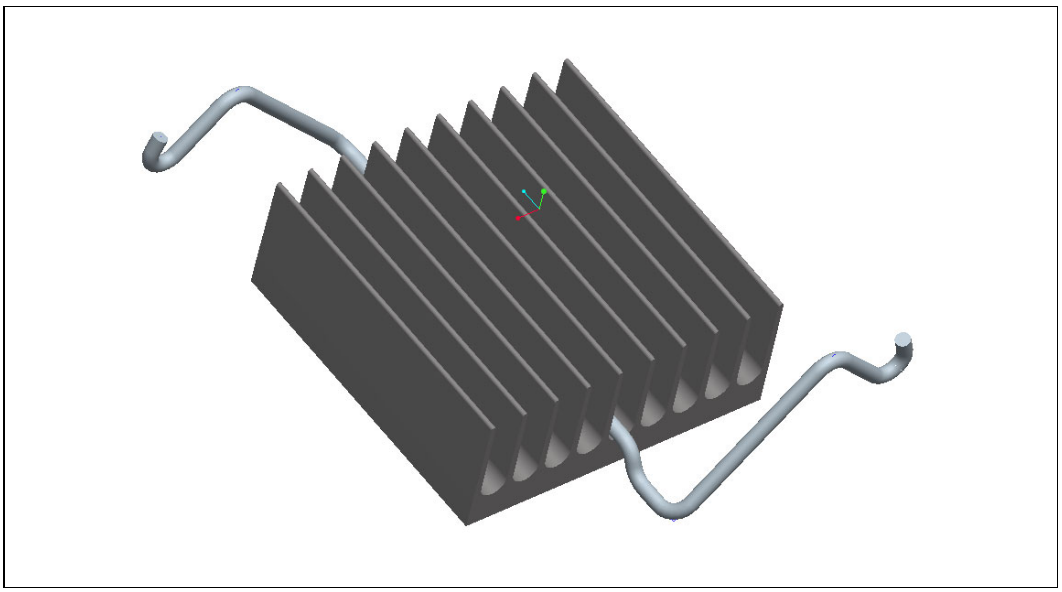


Figure 20. Intel® 6700PXH 64-Bit PCI Hub Reference Thermal Solution Assembly



6.4.1 Heat Sink Orientation

Since the MCH and PXH solutions are based on unidirectional heat sinks, mean airflow direction must be aligned with the direction of the fins of the heat sink.

6.4.2 Heat Sink Clip

The reference solutions use wire clips with hooked ends. The hooks attach to wire anchors to fasten the clip to the board. See Section 8.0 for mechanical drawings of the MCH and PXH clips.

6.4.3 Solder-Down Anchors

For platforms that have very limited board space, a clip retention solder-down anchor has been developed to minimize the impact of clip retention on the board. It is based on a standard three-pin jumper and is soldered to the board like any common through-hole header. A new anchor design is available with 45° bent leads to increase the anchor attach reliability over time. See Section 7.0 for the part number and supplier information.

6.4.4 Thermal Interface Material (TIM)

A thermal interface material provides improved conductivity between the die and heat sink. It is important to understand and consider the impact of the interface between the die and heat sink base on the overall thermal solution. Specifically, the bond line thickness, interface material area, and interface material thermal conductivity must be selected to optimize the thermal solution.

It is important to minimize the thickness of the thermal interface material (TIM), commonly referred to as the bond line thickness. A large gap between the heat sink base and the die yields a greater thermal resistance. The thickness of the gap is determined by the flatness of both the heat sink base and the die, plus the thickness of the thermal interface material, and the clamping force applied by the heat sink attachment method. To ensure proper and consistent thermal performance, the TIM and application process must be properly designed.

The MCH reference thermal solution uses Honeywell* PCM45F while the PXH reference thermal solution uses Chomerics* T-710. Alternative materials can be used at the users discretion. Regardless, the entire heat sink assembly, including the heat sink, TIM (including attach method), and the component (MCH or PXH) must be validated together for specific applications.

6.5 Reliability Requirements

Each motherboard, heatsink and attach combination may vary the mechanical loading of the component. The user should carefully evaluate the reliability of the completed assembly prior to use in high volume. Some general recommendations are shown in Table 5.

Table 5. Reliability Requirements

Test[1]	Requirement	Pass/Fail Criteria[2]
Mechanical Shock	50 g, board level, 11 ms, three shocks/axis	Visual Check and Electrical Functional Test
Random Vibration	7.3 g, board level, 45 min./axis, 50 Hz to 2000 Hz	Visual Check and Electrical Functional Test
Temperature Life	85 °C, 2000 hours total, checkpoints at 168, 500, 1000, and 2000 hours	Visual Check
Thermal Cycling	-5 °C to +70 °C, 500 cycles	Visual Check
Humidity	85% relative humidity, 55 °C, 1000 hours	Visual Check

NOTES:
1. The above tests should be performed on a sample size of at least 12 assemblies from three lots of material.
2. Additional Pass/Fail Criteria may be added at the discretion of the user.

7.0 Thermal Solution Component Suppliers

7.1 Intel® E7520/E7320 Chipset MCH Torsional Clip Heat Sink Thermal Solution

Part	Supplier	Part Number	Contact Information
Unidirectional Fin Heat Sink Assembly • Copper • Aluminum	Cooler Master*	Copper: Cooler Master part # ECB-00307-01-GP Intel part # D82056-001 Aluminum: Cooler Master part # ECB-00306-01-GP Intel part # D82052-001	Wendy Lin (USA) 510-770-8566, x211 wendy@coolermaster.com
Unidirectional Fin Heat Sink† • Copper • Aluminum	Cooler Master	Copper: Cooler Master Part # 250017230-GP Intel part # D82313-001 Aluminum: Cooler Master Part # 250017260-GP Intel part# D82309-001	Wendy Lin (USA) 510-770-8566, x211 wendy@coolermaster.com
Thermal Interface	Honeywell*	PCM45F	Paula Knoll 858-279-2956 paula_knoll@honeywell.com
Heatsink Attach Clip	CCI/ACK*	Intel part #: A69230-001	Harry Lin (USA) 714-739-5797 hlinack@aol.com Monica Chih (Taiwan) 866-2-29952666, x131 monica_chih@ccic.com.tw
	Foxconn*		Bob Hall (USA) 503-693-3509, x235 bhall@foxconn.com
Solder-Down Anchor	Foxconn	Foxconn part #: HB96030-DW Intel part #: A13494-005	Julia Jiang (USA) 408-919-6178 juliaj@foxconn.com

7.2 Intel® 6700PXH 64-Bit PCI Hub Torsional Clip Heat Sink Thermal Solution

Part	Supplier	Part Number	Contact Information
Heat Sink Assembly includes: • Unidirectional Fin Heat Sink • Thermal Interface Material • Torsional Clip	CCI/ACK*	Intel part #: C19228-001	Harry Lin (USA) 714-739-5797 hlinack@aol.com Monica Chih (Taiwan) 866-2-29952666, x131 monica_chih@ccic.com.tw
Undirectional Fin Heat Sink (31.0 x 31.0 x 12.2 mm)	CCI/ACK	Intel part #: C13084-001	Harry Lin (USA) 714-739-5797 hlinack@aol.com Monica Chih (Taiwan) 866-2-29952666, x131 monica_chih@ccic.com.tw
Thermal Interface	Chomerics*	Intel part #: 689850-001 Chomerics part #: 69-12-22066-T710	Todd Sousa (USA) 360-606-8171 tsousa@parker.com
Heatsink Attach Clip	CCI/ACK	Intel part #: C17725-001	Harry Lin (USA) 714-739-5797 hlinack@aol.com Monica Chih (Taiwan) 866-2-29952666, x131 monica_chih@ccic.com.tw
Solder-Down Anchor	Foxconn*	Intel part #: A13494-005 Foxconn part #: HB96030-DW	Julia Jiang (USA) 408-919-6178 juliaj@foxconn.com

8.0 Mechanical Drawings

Table 6 lists the mechanical drawings included in this appendix.

Table 6. Mechanical Drawing List

Drawing Description	Figure Number	Page Number
Intel® E7520/E7320 Chipset MCH Heat Sink Assembly	21	page 33
Intel® E7520/E7320 Chipset MCH Heat Sink	22	page 34
Intel® E7520/E7320 Chipset MCH Torsional Clip	24	page 36
Intel® 6700PXH 64-Bit PCI Hub Heat Sink Assembly	25	page 37
Intel® 6700PXH 64-Bit PCI Hub Heat Sink	26	page 38
Intel® 6700PXH 64-Bit PCI Hub Torsional Clip	27	page 39

Figure 21. Intel® E7520/E7320 Chipset MCH Heat Sink Assembly

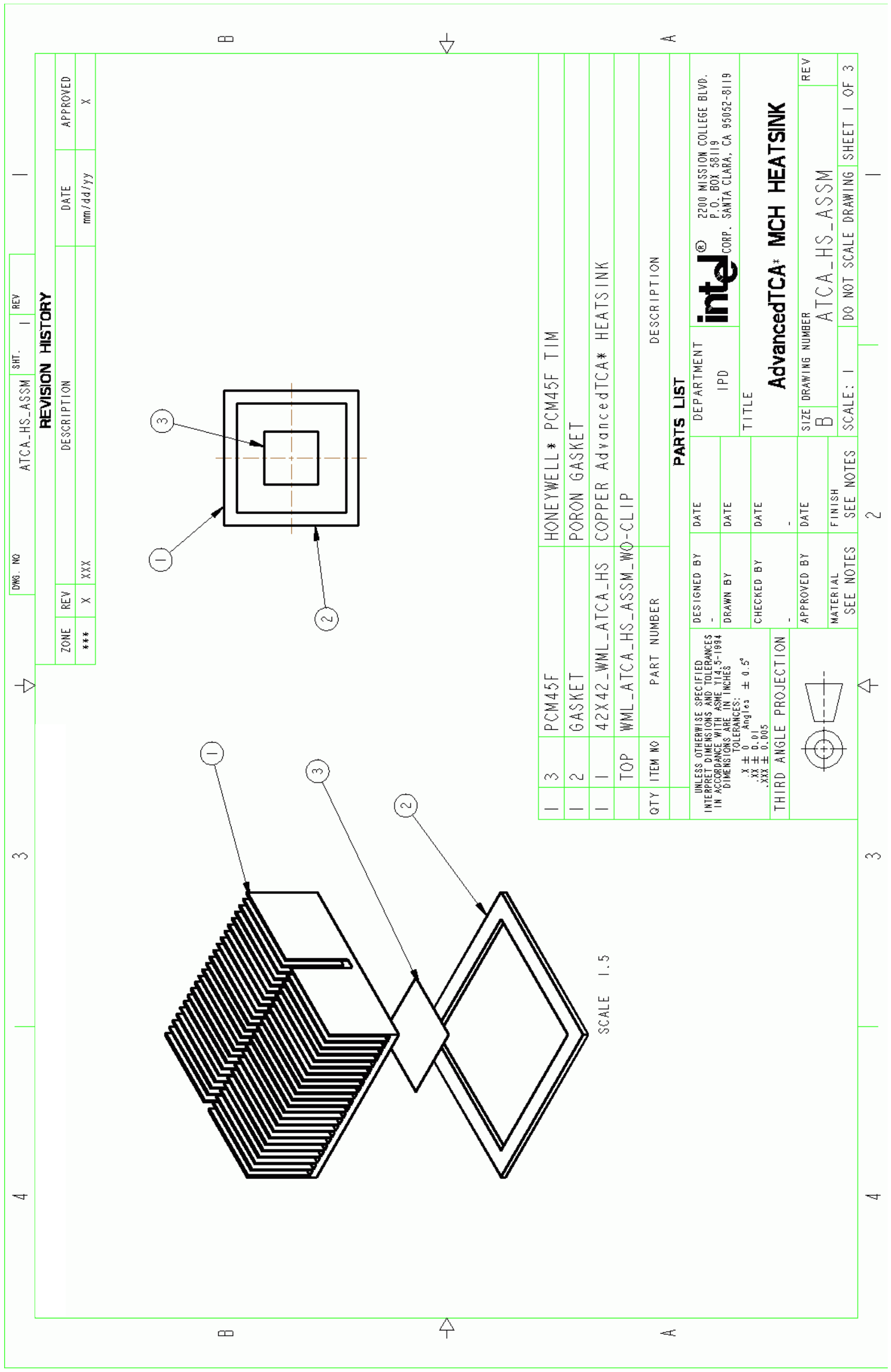


Figure 22. Intel® E7520/E7320 Chipset MCH Heat Sink

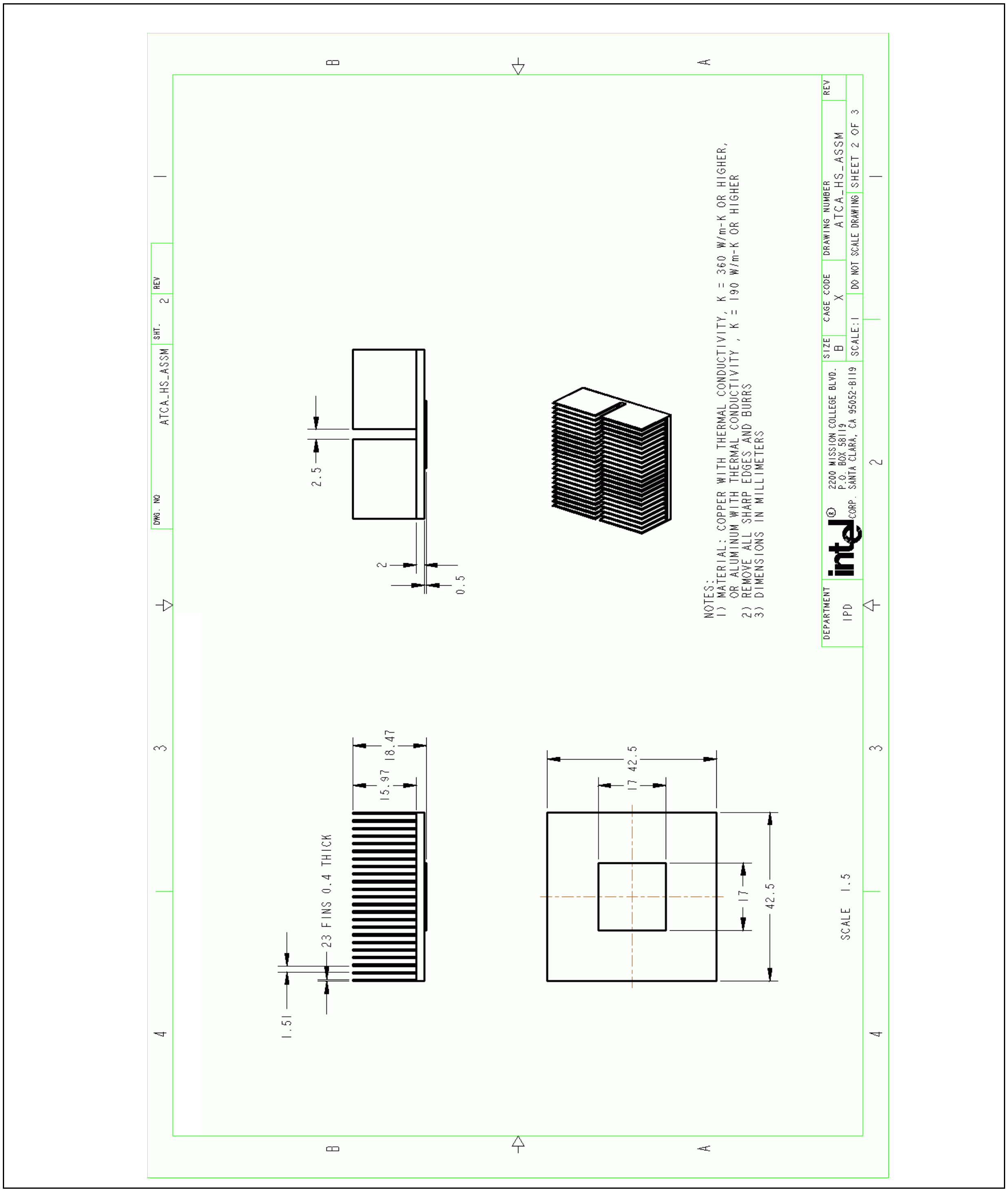


Figure 23. Intel® E7520/E7320 Chipset Gasket

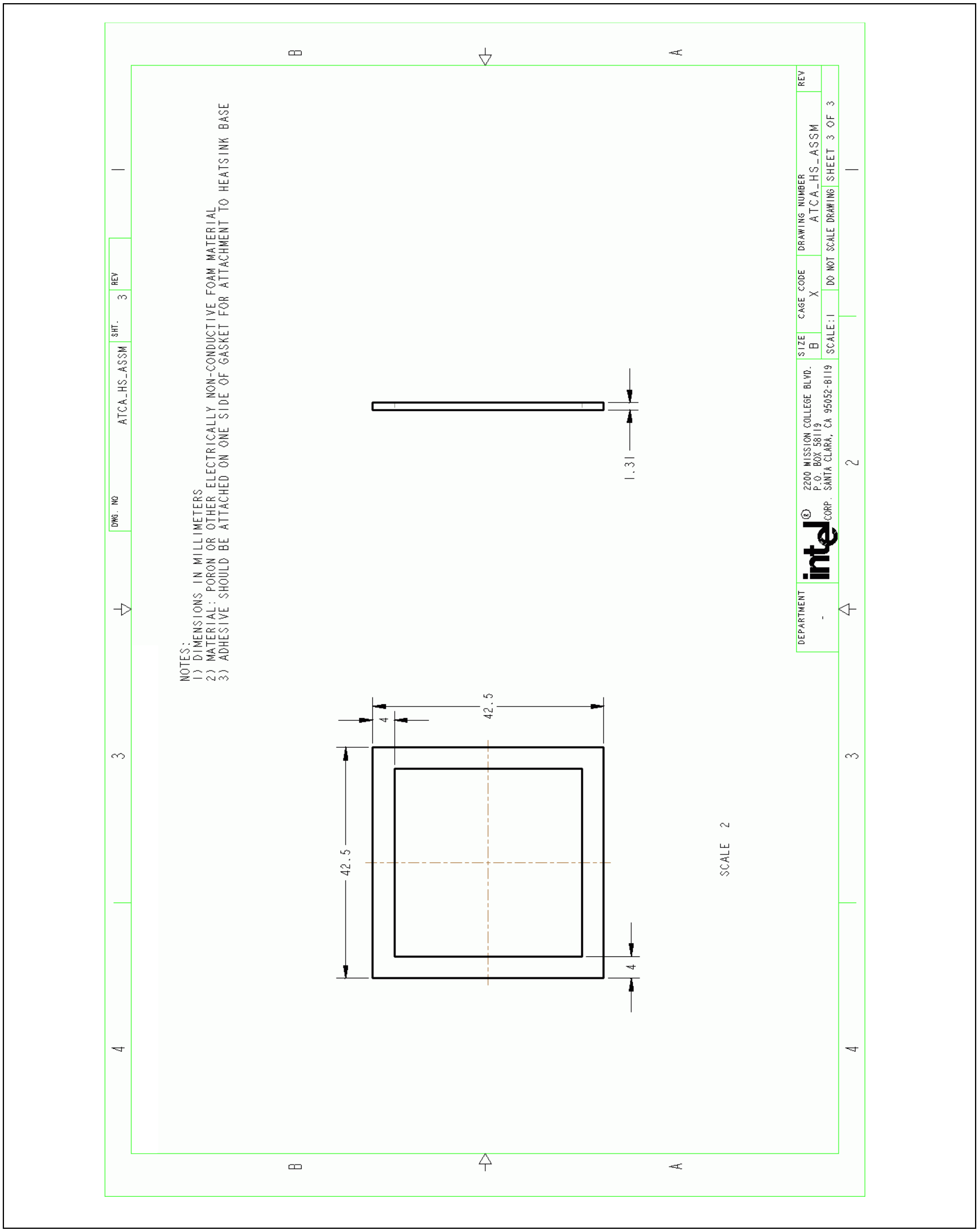


Figure 24. Intel® E7520/E7320 Chipset MCH Torsional Clip

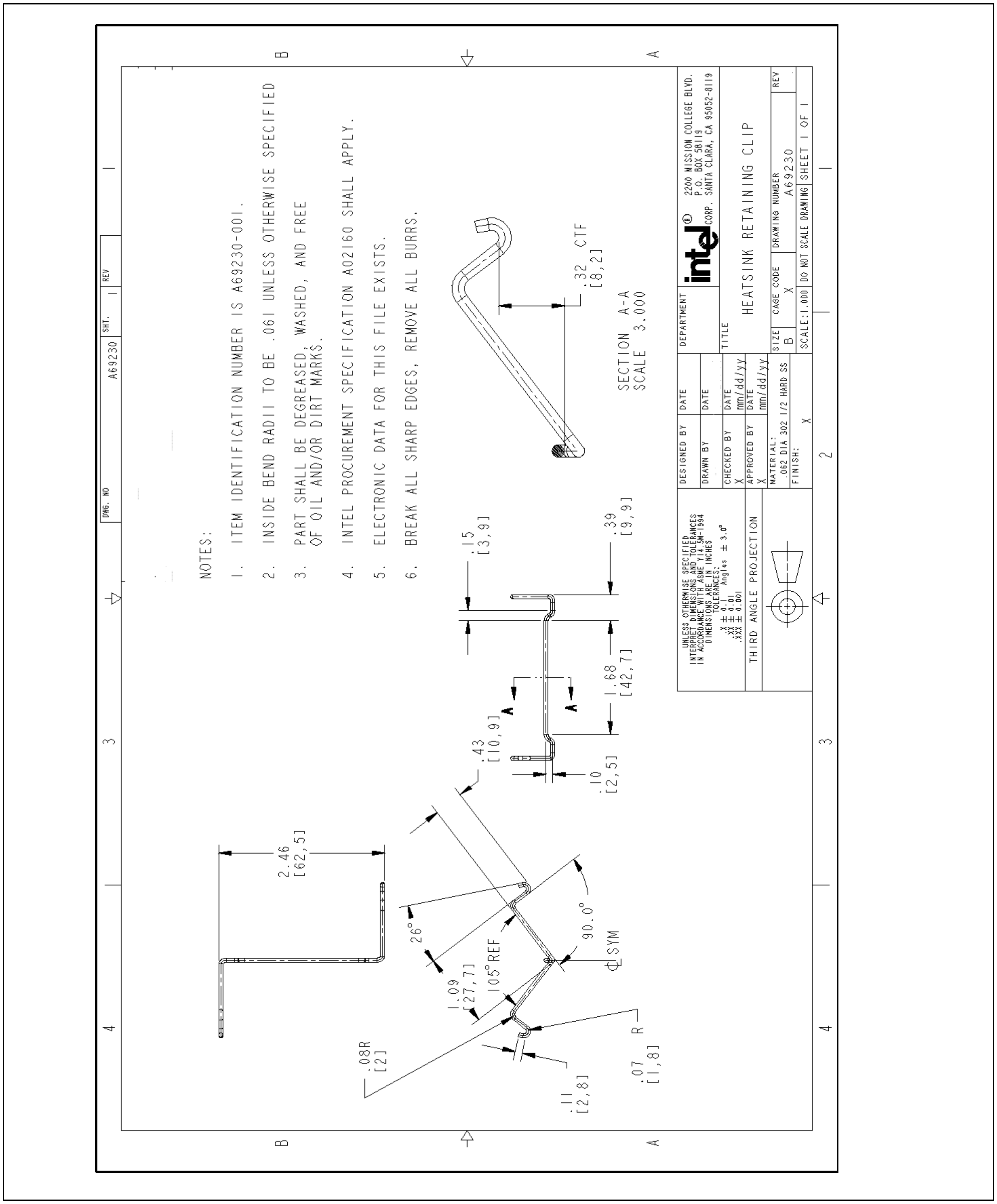


Figure 25. Intel® 6700PXH 64-Bit PCI Hub Heat Sink Assembly

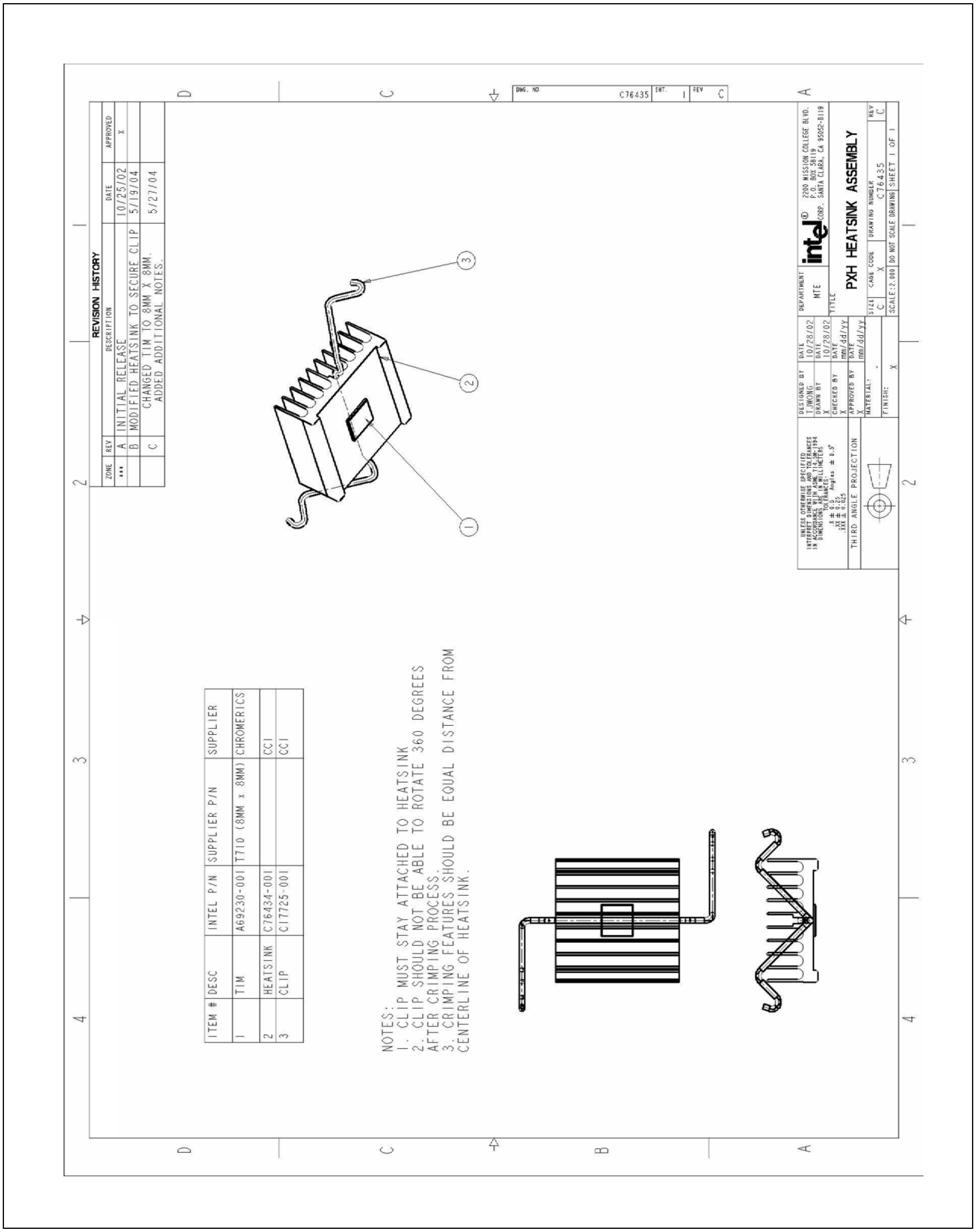


Figure 26. Intel® 6700PXH 64-Bit PCI Hub Heat Sink

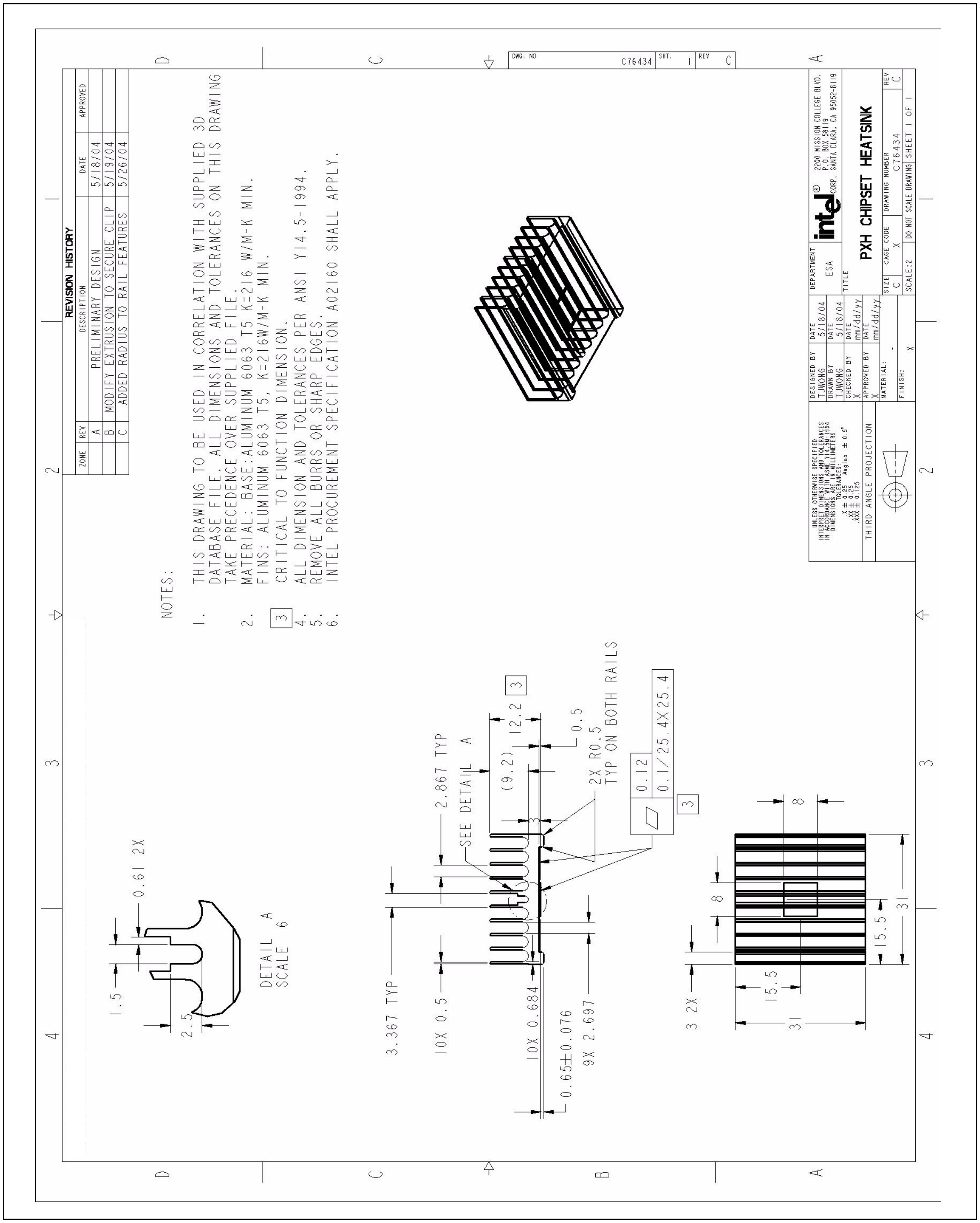


Figure 27. Intel® 6700PXH 64-Bit PCI Hub Torsional Clip